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LPVLSI Design - A Leakage Reduction Method for Portable Devices Using Cadence

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Abstract: Scaling of transistor features sizes has improves performance, increase transistor density and reduces the power consumption. As the threshold voltage is reduced due to scaling, it leads to increase in sub threshold leakage current and hence increase in static power dissipation. A chip's maximum power consumption depends on its technology as well as its implementation. As technology scales down and CMOS circuits are powered by lower supply voltages, standby leakage current becomes significant. In our daily life, miniaturised and compact electronic devices are integral components. All devices need charging some amount of time. In discharging time, devices are in inactive state. Why electronic devices are become battery discharge? Because of leakage current. Transistor size becomes smaller and smaller and also it becomes faster and faster because of high density and threshold voltage falls i.e.., leakage of current. As considered scaling of VLSI geometries, consumption of static power is more influencing than others. In the VLSI, demanding of scaling and static power. Designers using stacked sleep transistor without penalization in power setup, delay and performance in circuit.

Keywords: VLSI (very large scale integration), CMOS (complementary metal oxide semiconductor),sleep transistor, cadence virtuoso.

I. INTRODUCTION

Power consumption is one of the top concerns of Very Large Scale Integration (VLSI) circuit design, for which Complementary Metal Oxide Semiconductor (CMOS) is the primary technology. For reducing the power considered two main factors are area and speed. As the consequence, the design of an able to integrated circuit in status of power, area and speed as the same instant, it is become very difficult problem.

All portable electronic devices such as wireless applications contingent on the power dissipation as the most important factor for the reason of increasing rate of battery technology.

Implementation of low power circuit is a very important thought in present semiconductor technology. Today's portable electronic device has become to gain with effort better performance. Before designing engineers were give importance towards to performance and solidness of a design and give importance to design cost. As technology improving, engineers were more convergent on to bringing high speed circuits by minify the delay. As a year's across, IC'S become a very smaller, faster and usage of power consumption in many VLSI approaches but some changes in parameter values as well as process variations. In vey large scale integration, circuit designs are trade between power, area & performance. Low power design parameters of the below issues:

Source of power dissipation:

$P = P_{switching} + P_{short\ circuit} + P_{leakage} + P_{static}$

In this design, static power consumption is more dominant to reduce power dissipation in sleep transistor.

Where, $P = I_{static} . v$

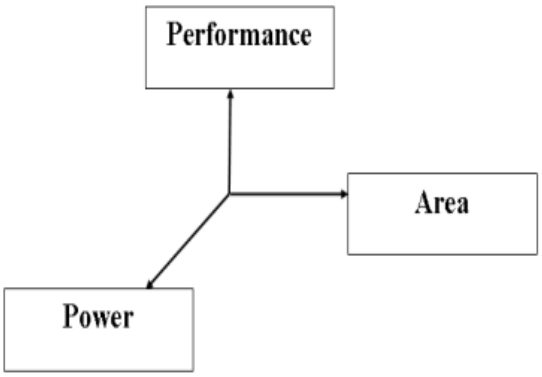

Fig.1 Parameters of VLSI

The concept of the sleep transistor is straight forward, optimal sleep transistor design and implementation are a challenge due to various effects, introduced by the sleep transistor and its implementations, on design performance, area, routability, overall power dissipation, and signal/power integrity. Optimal sleep transistor design also depends on design specific goals and chosen CMOS technology and process. A number of decisions need to be made including the choice of header or footer switch, normal or reverse body bias, optimal transistor size, and layout implementation details such as single or double row and extra rail or direct via-pillar for permanent power connection

Sub threshold leakage current (power) is becoming the primary source of power dissipation is CMOS. At smaller geometries, management of leakage current can greatly impact design and implementation choice. Till now, primary concerned were improving the performance of design and reducing silicon area to lower the cost. Now

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power is replacing performance as the key metric for VLSI design.

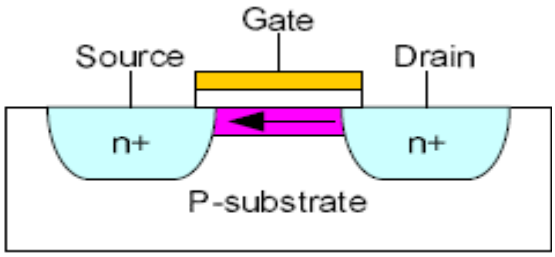

Fig.2: sub threshold leakage of an FET

One of the main contributors to static power consumption in CMOS is subthreshold leakage current shown in Figure 1, i.e., the drain to source current when the gate voltage is smaller than the transistor threshold voltage. Since subthreshold current increases exponentially as the threshold voltage decreases, nanoscale technologies with scaled down threshold voltages**.**

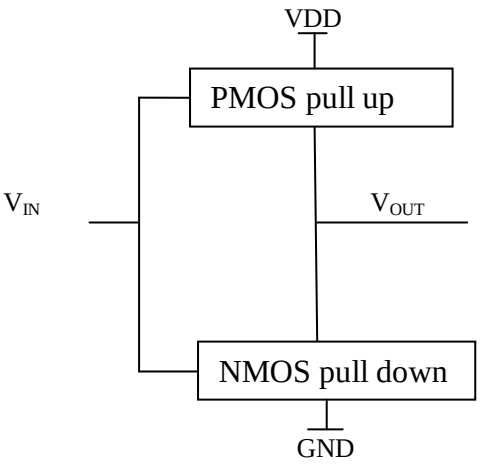

Fig.2: Basic CMOS

Above fig.2 shows the block diagram of digital circuit using conventional CMOS techniques. In this technique, a fully complementary CMOS circuit has an NMOS pull down network to connect the output to '0' (GND) and PMOS pull up network to connect the output to '1' (VDD). In this, output
Get dissipated in some time. So, avid this sleep transistor are added the above circuit as shown in below fig.3.

II. DESIGN IMPLEMENTATION

A sleep transistor is a circuit that performs both a PMOS or NMOS high threshold voltage transistor and it is used as a switch to turn off power supplies in standby mode as shown in below fig.3. The sleep transistor PMOS settled between Voltage of drain to drain and the pull up network hence it is called header switch and an additional sleep NMOS transistor Settled between voltage of source to source and pull down network hence it is called footer switch. In this technique happens is State destructive (outputs are floating when in sleep mode), Need retention circuitry, May be applicable for large digital blocks, Transistors with high Vth can be used

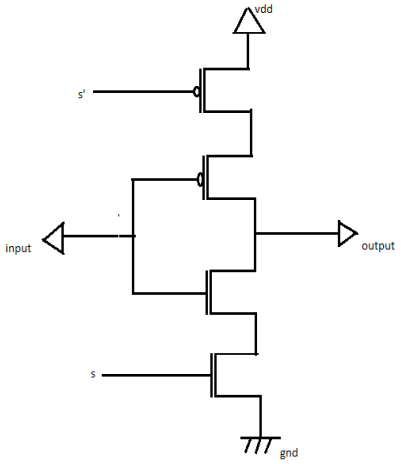

Fig.3: Schematic diagram of sleep transistor

The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors [5]. Figure 5 shows its structure. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active mode. However, area penalty is a significant matter for this approach since every transistor is replaced by three transistors and since additional wires are added for S and S‟, which are sleep signals

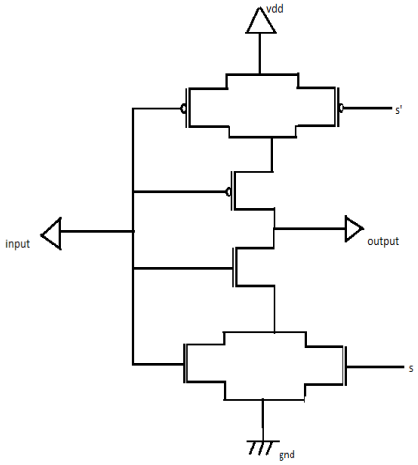

Fig.4: Schematic diagram of Forced stack

This approach explains the structure of the sleepy keeper approach [10] as well as how it operates. The basic problem with traditional CMOS is that the transistors are used only in their most efficient, and naturally inverting, way: namely, PMOS transistors connect to Vdd and NMOS transistors connect to Gnd .It is well known that PMOS transistors are not efficient at passing Gnd ; similarly, it is well known that NMOS transistors are not efficient at passing Vdd . However, to maintain a value of „1‟ in sleep mode, given that the „1‟ value has already been calculated, the sleepy keeper approach uses this output value of „1‟ and an NMOS transistor connected to Vdd to maintain output value equal to „1‟ when in sleep mode. As shown in fig 5.

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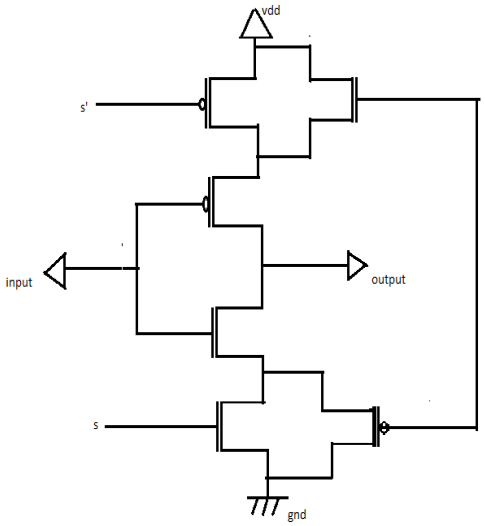

Fig.5: Schematic diagram of Sleepy keeper

However, area requirement is maximum for this technique since every transistor is replaced by three transistors.Dual sleep Technique[8] as shown in below figure. uses the advantage of using the two extra pull- up & pull-down transistors in sleep mode either in OFF/ON state. To all logic circuitry the dual sleep portion is designed as common. For a certain logic circuit less number of transistors are enough to apply

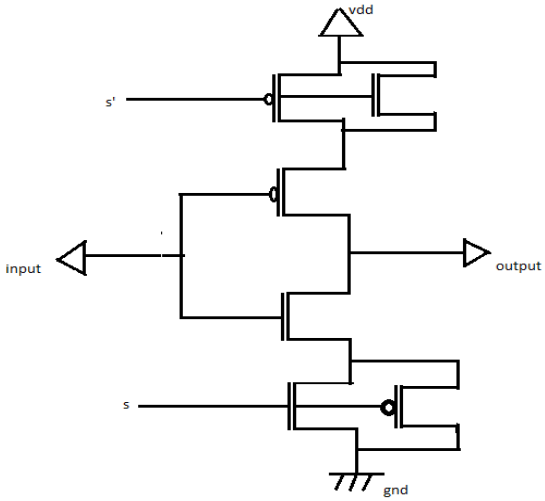

Fig.6: Schematic diagram of Dual sleep

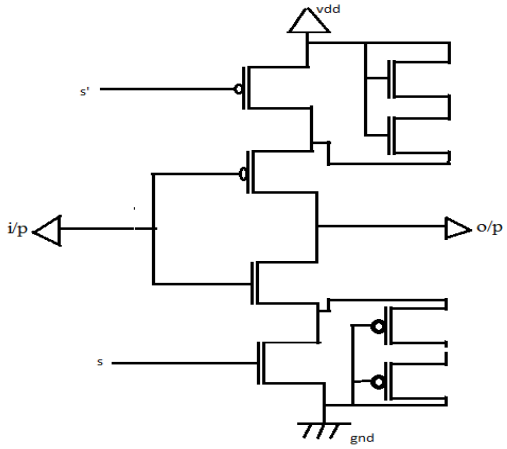

Fig.7: Schematic diagram of Dual stack

The method is dual stack approach [1], in sleep mode, the sleep transistors are off, i.e. transistor N1 andP1 are off. We do so by making S=0 and hence S'=1. Now we see that the other 4 transistors P2, P3 and N2, N3 connect the main circuit with power rail. Here we use 2 PMOS in the pull down network and 2 NMOS in the pull-up network. The advantage is that NMOS degrades the high logic level while PMOS degrades the low logic level. Due to the body effect, they further decrease the voltage level. So, the pass transistors decreases the voltage applied across the main circuit. Sub threshold leakage can be reduced by stacking transistors, i.e., taking advantage of the so-called "stack effect" [9]. The stack effect occurs when two or more stacked transistors are turned off together; the result is reduced leakage power consumption. The stacked sleep technique is compared with four of the techniques explained earlier namely; sleep transistor, sleepy stack, dual sleep and dual stack. Thus, five design approaches are compared in terms of power consumption, delay and power delay product. To show that the stacked sleep technique approach is applicable to general logic design a chain of 4 inverters is chosen. Spectre [11] was used for simulation purpose estimate delay power consumption.

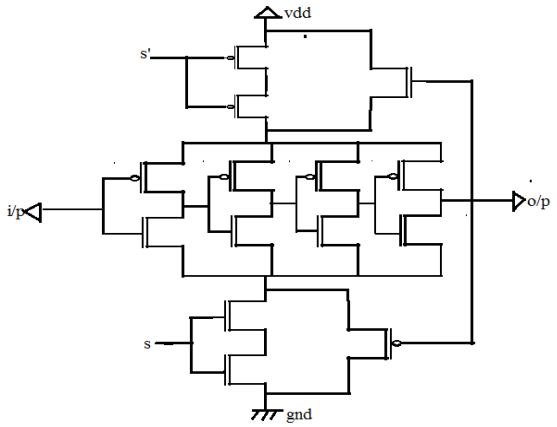

Fig.8: Schematic diagram of Proposed stacked sleep

III. SIMULATION RESULTST

A. The conventional method of sleep transistor:

1. Schematic diagram:

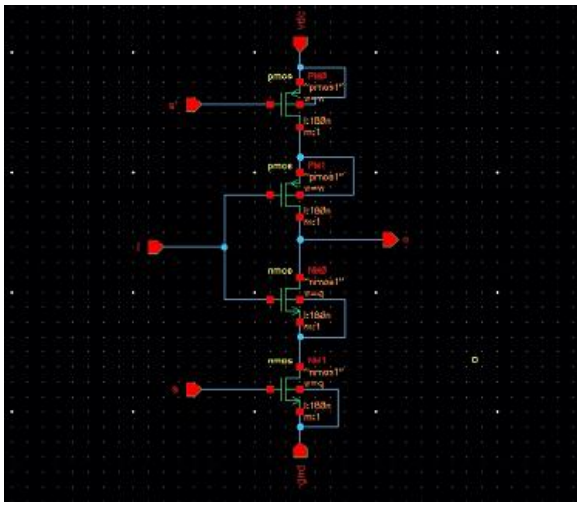
Fig.9: Schematic design of sleep transistor

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2. Test setup:

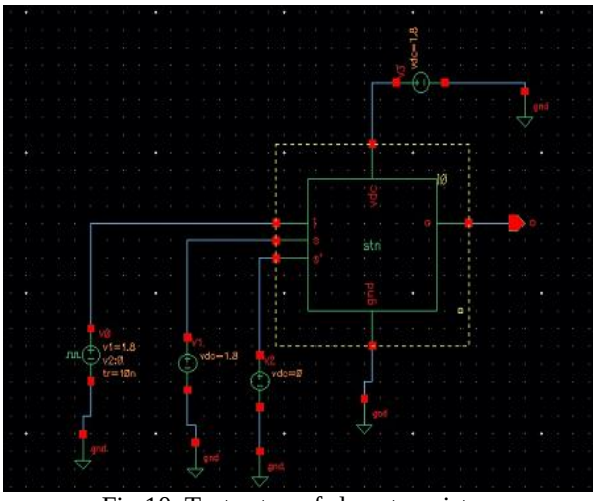

Fig 10: Test setup of sleep transistor

3. o/p waveform:

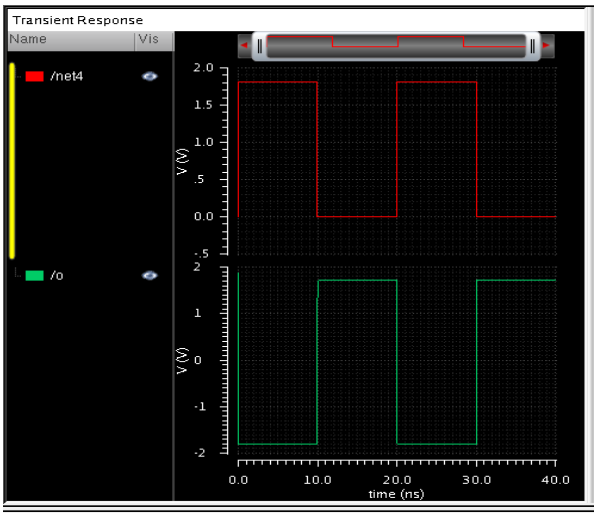

Fig.11: Output waveform of sleep transistor

4. Power analysis:

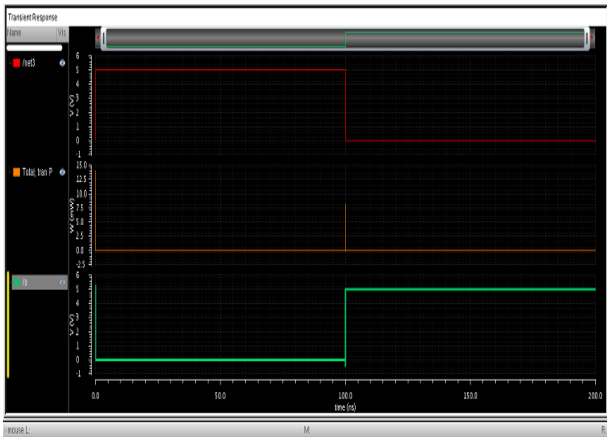

Fig.12: o/p waveform representing average power of sleep transistor

B. The conventional method of forced stack:

1. Schematic diagram:

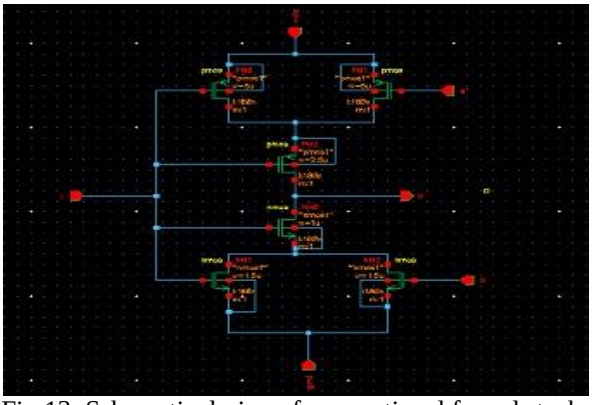

Fig.13: Schematic design of conventional forced stack

2. Test setup:

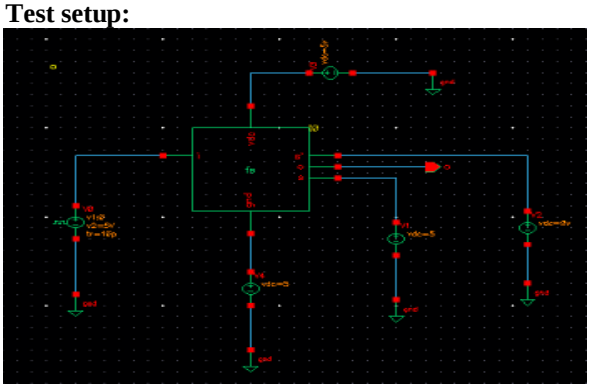

Fig.14: Test setup of conventional forced stack

3. o/p waveform:

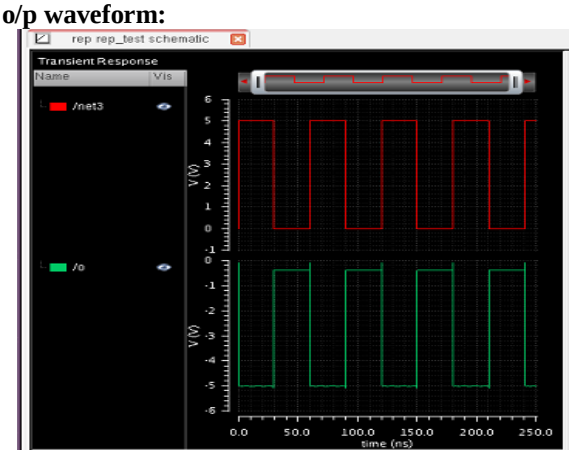

Fig.15: Output waveform of sleep transistor

4. Power analysis:

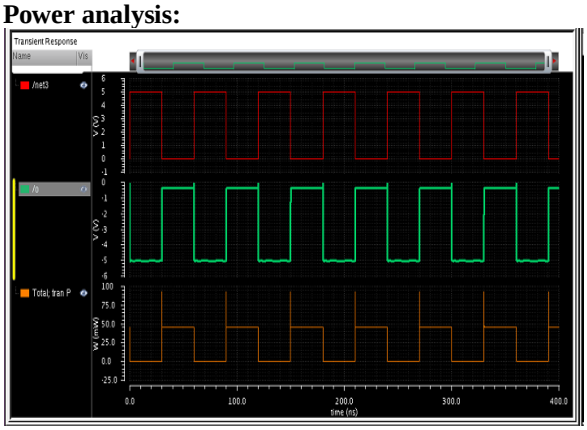

Fig.16: o/p waveform representing average power of sleep transistor

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C. The conventional method of sleepy keeper:

1. Schematic diagram:

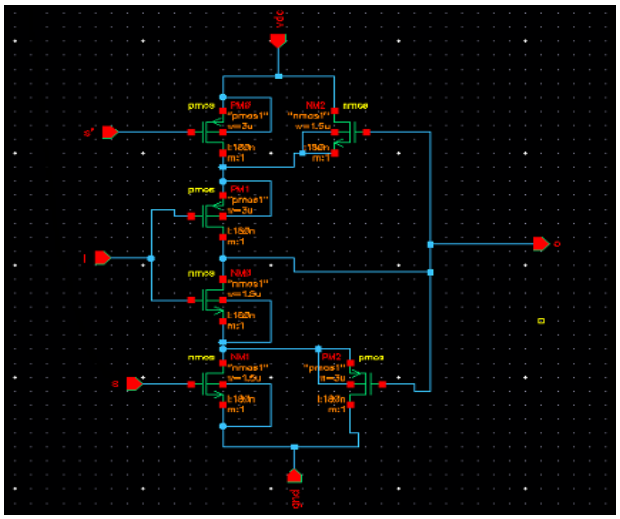

Fig.17: Schematic design of conventional sleepy keeper

2. Test setup:

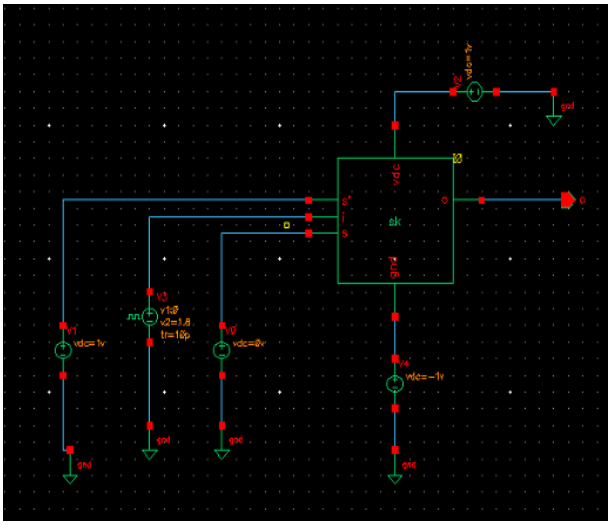

Fig.18: Test setup of conventional sleepy keeper

3. o/p waveform:

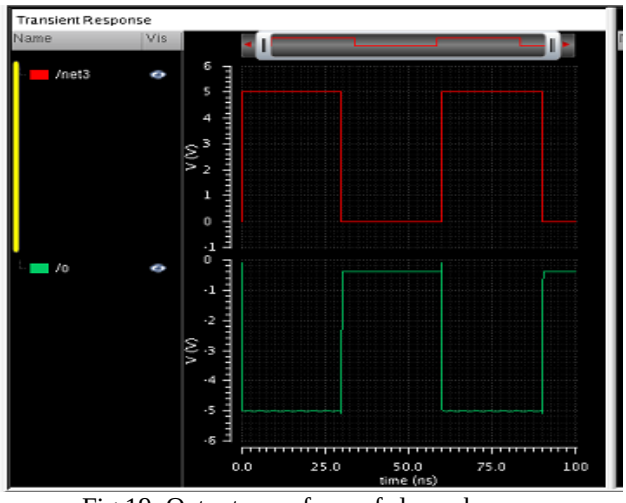

Fig.19: Output waveform of sleepy keeper

4. Power analysis:

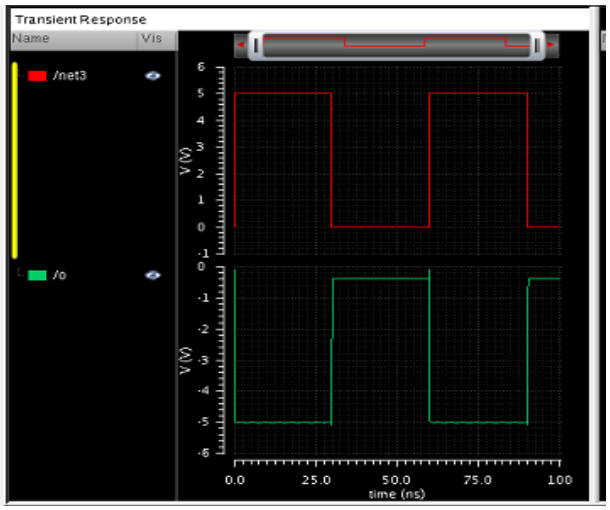

Fig.20: o/p waveform representing average power of sleepy keeper

D. The conventional method of dual sleep:

1.Schematic diagram:

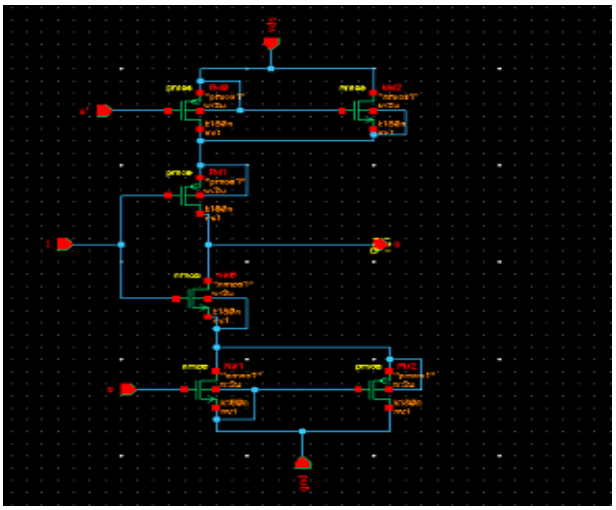

Fig.21: Schematic design of conventional sleepy keeper

2.Test setup:

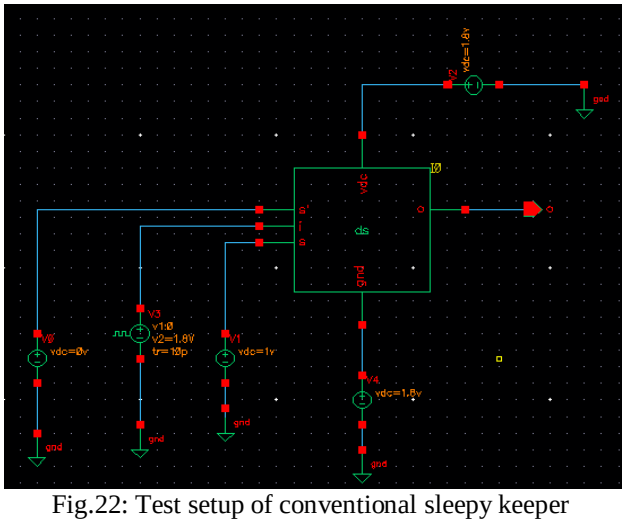

Fig.22: Test setup of conventional sleepy keeper

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3. o/p waveform:

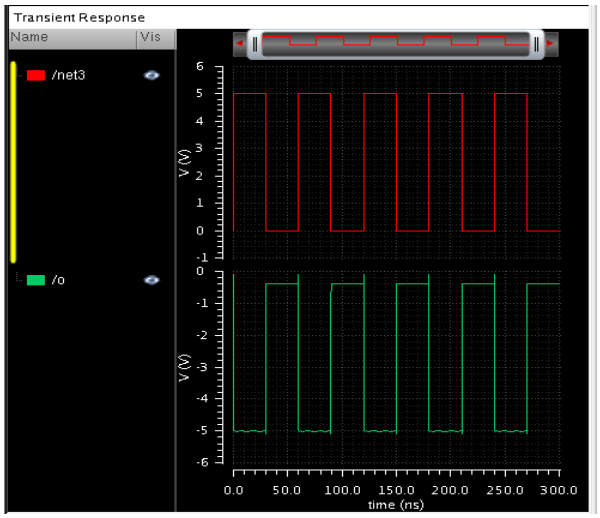

Fig.23: Output waveform of sleepy keeper

4. Power analysis

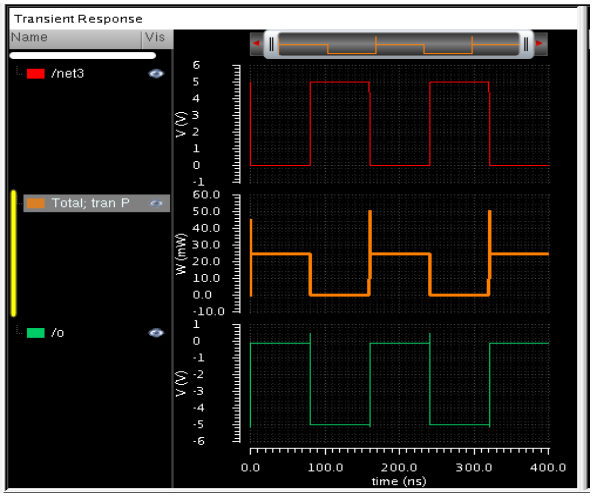

Fig.24: o/p waveform representing average power of sleepy keeper

D. The conventional method of dual sleep:
1.Schematic diagram:

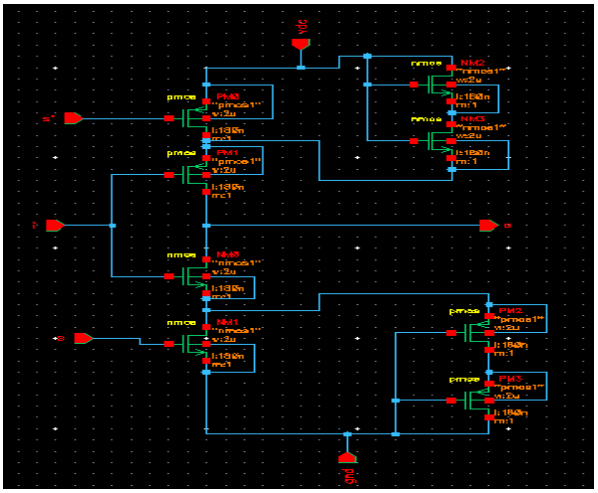

Fig.25: Schematic design of conventional sleepy keeper

2. Test setup:

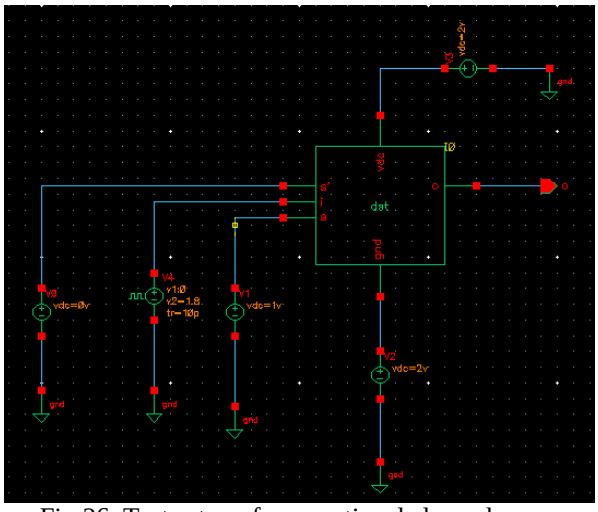

Fig.26: Test setup of conventional sleepy keeper

3. o/p waveform & power analysis:

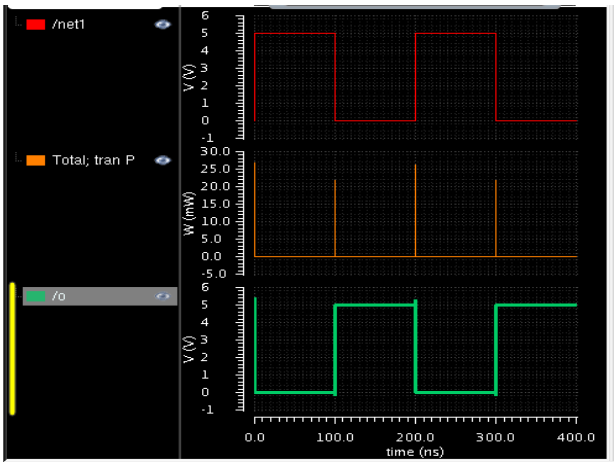

Fig.27: o/p waveform representing average power of sleepy keeper

2. Proposed method
A. Schematic diagram:

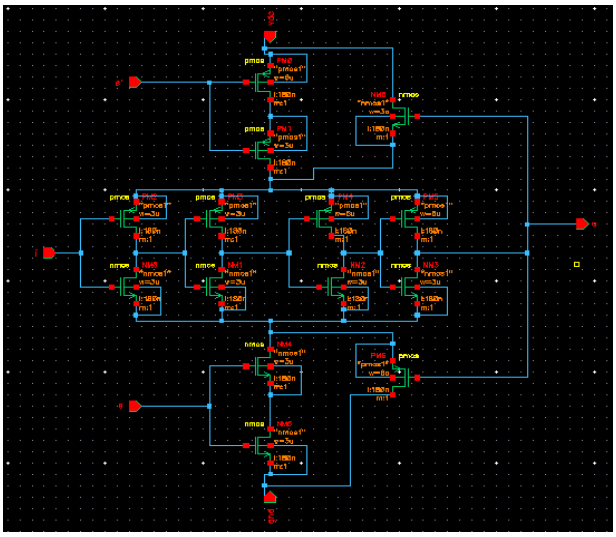

Fig.28: Schematic design of conventional sleepy keeper

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2.Test setup

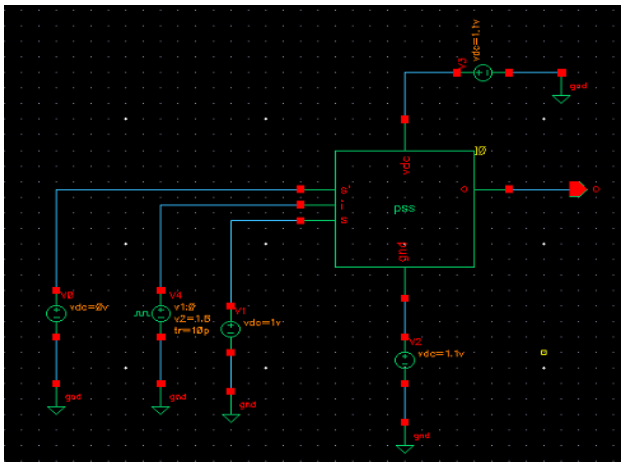

Fig.29: Test setup of conventional sleepy keeper

3. o/p waveform:

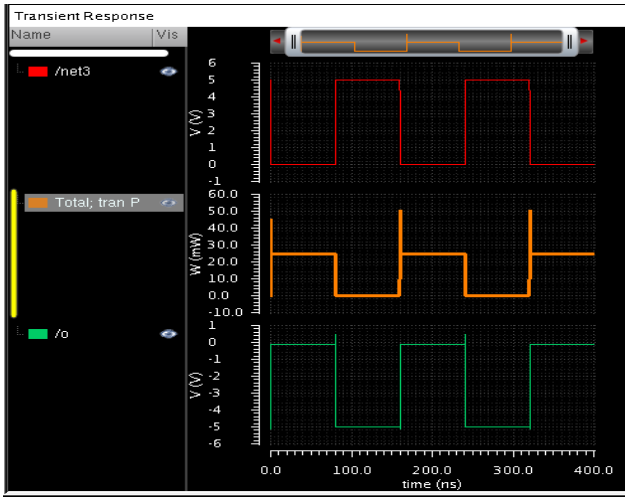

Fig.30: o/p waveform representing average power of sleepy keeper

3. Comparison between Power, Delay and PDP:

The following table gives Power, Delay, PDP values and its results of comparison.

Table 1: comparison between Power, Delay, PDP

Sl. no	Sleep transistors	Power (µW)	Delay (ns)	PDP(fJ)
1	Sleep transistor	2.124	12.36	26.252
2	Forced stack	5.197	16.37	85.074
3	Sleepy keeper	4.827	17.61	85.003
4	Dual sleep	4.794	17.41	83.463
5	Dual stack	4.823	17.72	85.463
6	Stacked sleep	2.226	100.0	22.26

From the comparison we can see that the stacked sleep transistor offers very good power reduction. But it suffers from delay. Nevertheless, in applications where delay can be compromised for low power, stacked sleep approach can be very useful.

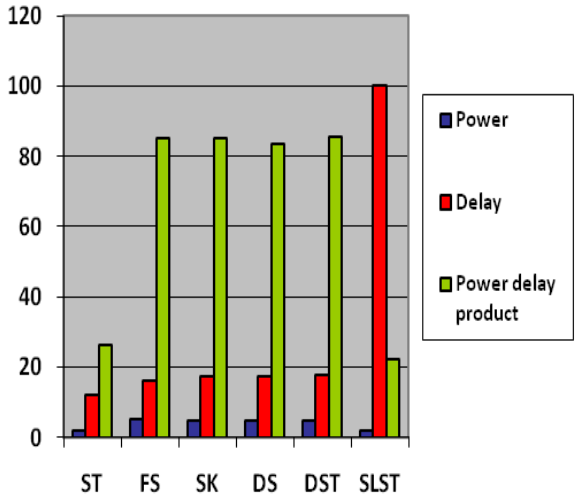

Fig.31:Bar chart representation of power, Delay and PDP

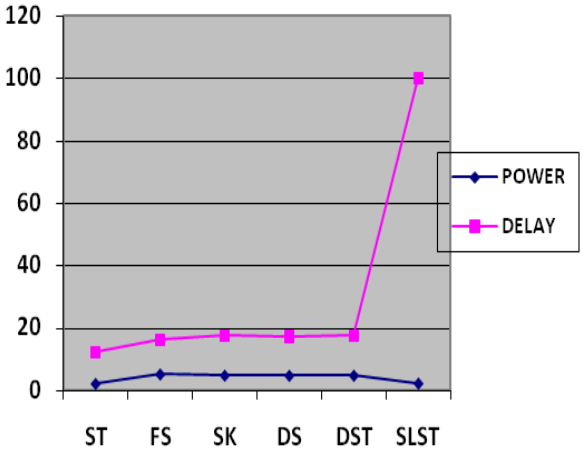

Fig.32: Comparison chart of power consumption and delay of different sleep transistors

Table 2: Comparison between Propagation delay and frequency

Sl. no	Sleep transistors	tp, Delay	2tp(ns)	Fmax=1/2tp (MHZ)
1	Sleep transistor	12.36	24.72	56.83
2	Forced stack	16.37	32.74	30.54
3	Sleepy keeper	17.61	35.22	28.39
4	Dual sleep	17.41	34.82	28.71
5	Dual stack	17.72	35.44	28.21
6	Stacked sleep	100	200	500

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Table 3: Comparison between Power consumption and frequency

Sl. no	Sleep transistors	Power consumption (μW)	Fmax=1/2tp (MXZ)
1	Sleep transistor	2.124	56.83
2	Forced stack	5.197	30.54
3	Sleepy keeper	4.827	28.39
4	Dual sleep	4.794	28.71
5	Dual stack	4.823	28.21
6	Stacked sleep	2.226	500

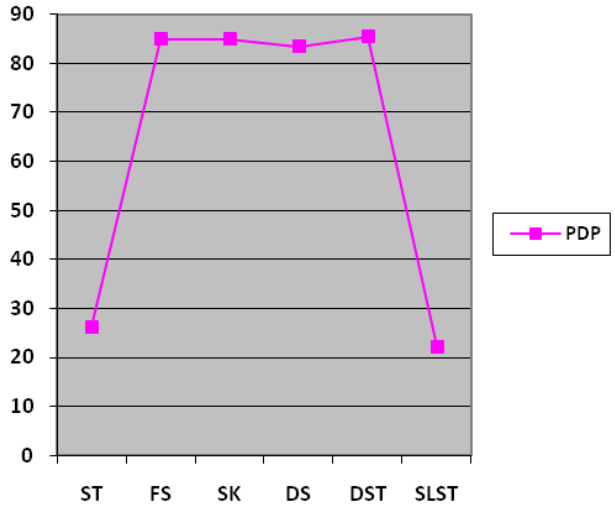

Fig33 : Power consumption versus switching frequency of different sleep transistor approaches

IV.CONCLUSION

This paper provides a brief analysis on different approaches of sleep transistor and their performance analysis. In the proposed design a new modified stacked sleep approach will be designed for sleep transistor applications. The slep transistor will be designed using Cadence Virtuoso 6.1.1 Version, Analog Design Environment. Simulations will be carried out on different techniques to obtain the best results. Power and Delay analysis is major area of concern.

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